In the Claims:

1. (Currently Amended) A method for forming a top oxide for a semiconductor ~~vertical transistor~~ device comprising a poly stud above a polysilicon fill in a deep trench and an isolation region in a portion of the deep trench, the method comprising the steps of:

~~forming an etch support~~ forming a nitride liner ~~by low pressure chemical vapor deposition~~ over the poly stud;

forming a support polysilicon over a portion of the isolation trench outside of an array;

depositing a top oxide over the semiconductor ~~vertical transistor~~ device;

forming a planarization coating over the top oxide; and

opening the poly stud~~, wherein the top oxide remains over a portion of the isolation trench~~.

2. (Original) The method of claim 1, further comprising forming a poly cap above the poly-stud above a polysilicon fill in a deep trench.

3. (Currently Amended) The method of claim 1, wherein ~~forming an etch support~~ forming a nitride liner further comprises forming implants.

4. (Original) The method of claim 3, wherein the implants are formed in a well, a support device, or both the well and the support device.

PAGE 5/11 * RCVD AT 12/14/2004 6:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08

5. (Original) The method of claim 1, further comprising performing a support gate oxidation prior to forming the support polysilicon, wherein the poly stud is protected from the support gate oxidation by the etch support nitride liner.

6. (Original) The method of claim 1, wherein the step of forming the support polysilicon further comprises:

depositing an etch array polysilicon over the memory device;

applying an etch array mask over a portion of the etch array polysilicon;

etching the etch array polysilicon; and

exposing a pad oxide on the substrate.

7. (Original) The method of claim 1, wherein the step of opening the polysilicon stud comprises:

applying a planarization coating; and

etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either high enough to clear the top oxide or, wherein the top oxide in the support can be removed using a mask.

8. (Original) The method of claim 1, wherein the step of opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon cap.

PAGE 6/11 * RCVD AT 12/14/2004 6:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08

9. (Original) The method of claim 1, wherein the step of opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating.

10. (Original) The method of claim 9, further comprising a timed etch oxide 1:1, removing a portion of the polysilicon cap.

11. (Currently Amended) A method for forming a top oxide for a vertical transistor device comprising the steps of:

providing a substrate;

forming a storage node in the substrate comprising a deep trench ~~filed~~ filled with a doped polysilicon;

forming a polysilicon stud above the doped polysilicon in the deep trench;

forming an isolation trench in an upper portion of the storage node and substrate;

forming a patterned etch support liner over a portion of the polysilicon stud, wherein the patterned etch support liner and the doped polysilicon fully encompass the polysilicon stud;

depositing a top oxide over the vertical transistor device;

forming a planarization coating over the top oxide; and

opening the stud to expose the polysilicon stud, wherein portions of the top oxide are preserved above the substrate and above the isolation trench.

12. (Original) The method of claim 11, wherein forming the isolation trench further comprises:

PAGE 7/11 * RCVD AT 12/14/2004 8:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08

forming a pad nitride over a portion of the deep trench memory device exposing a portion of the substrate and the polysilicon stud;

etching an isolation trench in the exposed portion of the substrate and the polysilicon stud;

filling the isolation trench with an insulating material;

removing the pad nitride to expose the substrate; and

performing an oxide deglaze.

13. (Original) The method of claim 11, wherein the step of opening the polysilicon stud comprises etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either high enough to clear the top oxide or, where the top oxide in the support can be removed by a mask.

14. (Original) The method of claim 11, wherein the step of opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon cap.

15. (Original) The method of claim 11, wherein the step of opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating.

16. (Original) The method of claim 15, further comprising a timed etch oxide 1:1, removing a portion of the polysilicon cap.

PAGE 8/11 * RCVD AT 12/14/2004 6:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08

17. (New) The method of claim 11, wherein forming a nitride liner comprises forming an etch support nitride liner.

18. (New) The method of claim 11, wherein forming a nitride liner comprises forming a nitride liner by low-pressure chemical vapor deposition.

19. (New) The method of claim 11, wherein the semiconductor device comprises a vertical transistor device.

20. (New) The method of claim 11, wherein opening the poly stud comprises opening the poly stud such that the top oxide remains over a portion of the isolation region.

21. (New) The method of claim 11, wherein the deep trench is formed in a semiconductor body and wherein opening the poly stud comprises opening the poly stud such that the top oxide remains over the semiconductor body adjacent the deep trench.

22. (New) A method of forming a semiconductor device, the method comprising:

forming a trench in a semiconductor body;

forming a conductive stud in at least an upper portion of the trench;

forming an isolation region in at least the upper portion of the trench adjacent the conductive stud;

forming a liner over the conductive stud;

PAGE 9/11 * RCVD AT 12/14/2004 6:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08

forming a conductor over the trench so that the conductor overlies the conductive stud and the isolation region;

removing a portion of the conductor over the conductive stud;

depositing a top insulator over the semiconductor body including over the isolation region, the conductive stud, and remaining parts of the conductor;

forming a planarization layer over the top insulator; and

removing portions of the top insulator and the planarizing layer so as to expose an upper surface of the conductive stud.

23. (New) The method of claim 20 wherein:

the conductive stud comprises a polysilicon stud;

the liner comprises a nitride liner;

the conductor comprises polysilicon; and

the top insulator comprises an oxide.

PAGE 10/11 * RCVD AT 12/14/2004 6:25:15 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9727329218 * DURATION (mm-ss):03-08